Nanodevices and Their Operation Principles

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Abstract:

The objective of the lectures on: "Nanodevices and Their Operation Principles" is to introduce Ph. D. course students from different departments of our University into state of the art in construction and operation of nanometer-scale transistors for integrated circuits. A further objective is to introduce them into known physical, construction and material issues that limit further miniaturization and improvement of operation speed of the devices and require solutions in the coming years.

Course syllabus:

1. Brief introduction to operation and construction of integrated Si MOSFETs: simplified operation principle, simplified fabrication process.
2. Scaling down field effect transistors in CMOS integrated circuits –state of the art: effect of scaling down on operation speed and packing density; rules of MOSFET scaling and their applicability; evolution of constructions of nano-transistors in contemporary integrated circuits – down to 20-nm transistors; main technological limitations to further scaling; proposed methods to overcome them.
3. Generic idea of a transistor: a device with two reservoirs of electrical carriers and a potential barrier controlling flow of a current; a picture of a transistor as a device composed of "building blocks"; examples of transistors operating with different principles and constructed of different blocks.
4. Resume of physics used in classical drift-diffusion formalism applied for analysis of Si MOSFETs: energy bands, carrier concentrations, carrier generation and recombination, drift and diffusion as carrier transport mechanisms.
5. Device "building blocks": metal-semiconductor contacts; pn-junctions, heterojunctions; creation of controlled barriers of potential with pn junctions, heterojunctions and field effect.
6. MOSFET drift-diffusion physics: MOS structure and capacitance, threshold voltage, current-voltage characteristics, short-channel effects, mobility degradation, velocity saturation, tunneling in MOS structure.
7. Short-channel and thin gate dielectric effects in nanometer-scale MOSFETs: Tri-gate field effect transistors (FinFETs) and ultra-thin body Si on insulator MOSFETs as solutions to some short-channel effects in bulk Si MOSFETs; gate dielectric thickness and material choice effect on performance of transistors.
8. Physical limits of operation of less than 10-nm MOSFETS: effects a distance between doping atoms comparable with channel length; fundamental limitations arising from uncertainty principle and from thermodynamics.
9. Possibility of ballistic transport of electrons in short-channel transistors: theory of ballistic

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electron flow in semiconductors; electron scattering as a limiting mechanism.

10. Electron tunneling as electric charge carrier flow mechanism in ultra-short transistors: calculation methods of tunneling currents, direct and indirect tunneling.

11. Low dimensional structures: quantum wells, quantum wires, quantum dots – effect of low dimensionality on density of states and current conduction; applications to MOSFETs, memories and lasers.

12. Case study: operation of GaAs based 10-nm static induction transistor with direct tunneling and ballistic motion as current conduction mechanisms.

13. Two-dimensional materials, graphene and MoS2, for future nano-transistors - hope and difficulties in development of devices.

TERMINY WYKŁADÓW			
Data	**Dzień tygodnia**	**Godzina**	**Sala**
18-11-2013	Poniedziałek	15-18	105 NE (Nowy Gmach WETI)
25-11-2013	Poniedziałek	16-18	105 NE (Nowy Gmach WETI)
02-12-2013	Poniedziałek	16-18	105 NE (Nowy Gmach WETI)
09-12-2013	Poniedziałek	16-18	105 NE (Nowy Gmach WETI)
16-12-2013	Poniedziałek	16-18	105 NE (Nowy Gmach WETI)
13-01-2014	Poniedziałek	16-18	105 NE (Nowy Gmach WETI)
20-01-2014	Poniedziałek	16-18	105 NE (Nowy Gmach WETI)

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